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NOISE CANCELLATION IN MIXED SIGNAL ENVIRONMENT

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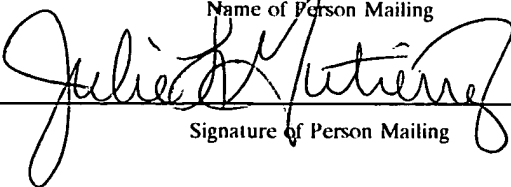
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NOISE CANCELLATION IN MIXED SIGNAL ENVIRONMENT

BACKGROUND OF THE INVENTION

Field of the Invention

5 The present invention generally relates to the art of processing electrical signals. In particular, the present invention relates to the art of noise cancellation in analog circuits.

Description of Related Art

10 Many integrated circuit (IC) devices include both digital circuits and analog circuits. Such an IC is referred to as a mixed-signal integrated circuit (MSIC). The application of the MSIC is most prevalent for IC's used in the multimedia and communications devices such as wireless communication systems, or cellular telephones. Even in mostly digital circuit IC's, analog circuits are used to achieve functions not realizable or difficult to implement using purely digital circuits.

15 Even though the use of analog circuits may be advantageous in many designs, the IC industry has been attempting to minimize the use of analog circuits for IC chips having digital circuits because of the susceptibility of the analog circuits to noise generated by the digital circuits. Digital circuits, especially the larger digital circuits prevalent in the industry, are very noisy relative to typical analog circuits surrounding the digital circuit. The analog circuits may fail due to
20 the noise generated by the digital circuits.

Moreover, increasing miniaturization of electronic devices, especially in the communications market, has required the IC chips to become even more tightly integrated. Consequently, the circuits comprising the IC chips, both digital and analog, are being fabricated close to each other, thereby aggravating the negative

effects of the noise.

Previous attempts to alleviate the problem focused on the method of shielding circuit blocks of an IC or focused on isolating the circuits of the IC. For example, the United States Patent Number 4,628,343, entitled "Semiconductor Integrated Circuit Device Free From Mutual Interference Between Circuit Blocks Formed Therein," issued to Yuji Komatsu, discloses an IC where "the first and second circuit blocks are shielded electrically from each other on the surface of the semiconductor chip." Col. 2 ll. 27-30, the Komatsu reference. In the United States Patent Number 5,453,713, entitled "Noise-Free Islands in Digital Integrated Circuits," issued to Hamid Partovi and Andrew J. Barber, the "integrated circuit chip has both digital and analog circuit functions, with one or more islands for isolating the analog functions from noise caused by the digital functions." Abstract, the Partovi and Barber reference. However, in tightly integrated, compact IC packages, shielding or isolation techniques may not be desirable, sufficient, or even feasible.

SUMMARY OF THE INVENTION

These problems are addressed by apparatuses and methods according to the present invention.

According to one embodiment of the present invention, there is provided a circuit comprising a first analog circuit, a second analog circuit, and a third circuit. An input signal is processed by the first circuit and results in an output signal which is the function of the first circuit and noise. The second analog circuit is configured to produce the noise component of the output signal from the first circuit. The third circuit is used to subtract the noise component from the output signal from the first circuit, resulting in the noise-free signal.

In order for the second circuit to produce a similar noise signal compared

to the noise component of the first circuit, the second circuit is placed proximal to the first circuit. Also, the noise cancellation techniques of the present invention are most useful in mixed signal environments where analog and digital circuits are located near each other.

5 According to another embodiment of the present invention, there is provided a circuit comprising a first analog circuit, a second analog circuit, and a third circuit. An input signal is processed by the first circuit and results in an output signal which is the function of the first circuit and noise. The second analog circuit is configured to produced a signal which is inverse of the output of
10 the first circuit. The third circuit is used first to subtract the output from the second circuit from the output signal from the first circuit, and second to halve the resultant. Then, the final output from the third circuit is the noise-free output portion of the first circuit.

15 The above-summarized techniques can be applied to multiple analog circuits.

20 According to another embodiment of the invention, a noise cancellation method is disclosed. First, an input signal is supplied to a first analog circuit. Second, the output from the first circuit is read. Third, a null input signal is supplied to a second analog circuit located proximal to said first analog circuit. Fourth, the output from the second analog circuit is read. Finally, the two outputs are combined to produce a signal which is the first output signal without the noise component.

25 These and other aspects, features, and advantages of the present invention will be apparent to those persons having ordinary skilled in the art to which the present invention relates from the foregoing description and the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram illustrating an embodiment of the present invention;

FIG. 2 is a block diagram illustrating another embodiment of the present invention;

FIG. 3 is a block diagram illustrating yet another embodiment of the present invention; and

FIG. 4A is a block diagram illustrating a digital subtractor; and

FIG. 4B is a block diagram illustrating an analog subtractor.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT(S)

Referring to the drawings, particularly to Fig. 1, a first analog circuit 10 processes input signal 11, denoted S_{11} , and produces an output signal 15, S_{15} . The function of the first circuit 10 can be represented as:

$$S_{15} = F_{10}(S_{11})$$

where S_{nn} represents the signal for the line nn and F_{nn} represents the function of circuit nn . This output signal $F_{10}(S_{11})$, a function of the input signal 11, S_{11} , as processed by the first circuit 10, is the desired output of the circuit 10. However, due to noise, especially from a noisy digital circuit 16 in this case, the actual output of the circuit 10, at signal line 15, is:

$$S_{15} = F_{10}(S_{11}) + N_{10}$$

where N_{10} is the noise component at the signal line 15 and represents the unwanted signal produced by circuit 10 due to the effects of the noise. Here, N_{nn} represents the noise component of the output signal of circuit nn .

B The digital circuit 16 can be, but not necessarily, connected to the first circuit.

5 The second circuit 12 and the third circuit 14 is provided to eliminate the effect of the noise, N_{10} , of the circuit 10, thereby producing the desired, a noise free, signal $F_{10}(S_{11})$ as the output at line 19.

Implementation 1

10 To eliminate the noise, N , a second analog circuit 12 and a third circuit 14 are added. The second circuit 12 is typically identical in design to the first circuit 10 and placed proximal to the first circuit 10 so as to experience the same noise affecting the first circuit 10. However, the input signal 13, S_{13} , to the second circuit 12 is designed to produce a *null output* relative to the circuit. A null output of the second circuit 12 is an output, absent the effects of noise, which can be added to or subtracted from the output of the first circuit 10 without effecting the value of the output of the first circuit. The null output may mean a zero voltage output as the output signal line 17, S_{17} , a zero current output signal S_{17} , or any other output which, when added to or subtracted from output signal 15, will not change the signal 15. To simplify the discussion, the null output will be assumed to be zero. Alternatively expressed, we design the second input signal 13 to produce an output signal 17 such that

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$$S_{17} = F_{12}(S_{13}) = 0 = \text{zero}.$$

Because the second circuit 12 is an identically designed circuit to the first circuit 10, the function of the second circuit, F_{12} , is identical in design to the function of the first circuit, F_{10} . Alternatively expressed,

$$F_{10} = F_{12}.$$

25 However, as with the first circuit 10, the effect of the noise will produce the

following output signal 17, therefore, the actual value of the signal at line 17, S_{17} is:

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$$\begin{aligned} S_{17} &= F_{12}(S_{13}) + N_{12} \\ &= 0 + N_{12} \\ &= N_{12}. \end{aligned}$$

Therefore, the second circuit 12 may also be called a noise separator circuit.

Because the second circuit 12 is identical in design to the first circuit 10, and because the second circuit 12 experiences the same noise as the first circuit, the noise N_{12} can be equated to N_{10} ,

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$$N_{10} = N_{12}.$$

The third circuit 14 subtracts the output signal 17 from the output signal 15 to produce the desired, a noise free output of the function F_{10} in response to signal S_{11} , $F_{10}(S_{11})$. Alternatively, the function of the third circuit 14 can be expressed as follows:

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$$\begin{aligned} S_{19} &= \text{the output signal 19 of the third circuit 14} \\ &= S_{15} - S_{17} \\ &= (F_{10}(S_{11}) + N_{10}) - N_{12} \quad ; \text{ note } N_{10} = N_{12} \\ &= F_{10}(S_{11}) + N_{10} - N_{10} \\ &= F_{10}(S_{11}). \end{aligned}$$

20 Accordingly, the final resultant signal, S_{19} , is the result of the original operations of the first circuit 10 on the input signal 11, $F_{10}(S_{11})$.

If the outputs of the first circuit 10 and the second circuit 12 are analog signals, an analog subtractor may be used. Analog subtractors are well known in the art, and Fig. 4B illustrates a simple analog subtractor 120. Referring to Fig. 25 4B, the incoming signal, I, 122 is inverted by the Op. Amp. 124 to produce, as the

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Toos!

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$$\begin{aligned} &= (F_{10}(S_{11}) + N_{10}) - (-F_{10}(S_{11}) + N_{10}) \\ &= F_{10}(S_{11}) + N_{10} + F_{10}(S_{11}) - N_{10} \\ &= F_{10}(S_{11}) + F_{10}(S_{11}) \end{aligned}$$

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$$\begin{aligned} &= (F_{10}(S_{11}) + N_{10}) - (-F_{10}(S_{11}) + N_{10}) \\ &= F_{10}(S_{11}) + N_{10} + F_{10}(S_{11}) - N_{10} \\ &= F_{10}(S_{11}) + F_{10}(S_{11}) \end{aligned}$$

$$= 2F_{10}(S_{11}).$$

The resultant signal, S_{19} , is the two (2) times the result of the original operations of the first circuit 10 on the input signal 11.

If the third circuit 14 further comprises circuits to half the resultant signal, then

$$\begin{aligned} S_{19} &= S_{15} - S_{17} && ; \text{ see above for operations} \\ &= 2F_{10}(S_{11}) / 2 \\ &= F_{10}(S_{11}). \end{aligned}$$

Again, the final resultant signal, S_{19} , is the result of the original operations of the first circuit 10 on the input signal 11, $F_{10}(S_{11})$.

Implementation 3

For multiple analog circuits exposed to the same environment, a single noise separator circuit can be utilized to remove the noise component of multiple analog circuits. Referring now to Fig. 2, a plurality of analog circuits 20, 22, 24, and 28 are illustrated. The inputs for the circuits 20, 22, 24, and 28 are provided by lines 21, 23, 25, and 29, and are designated as signals S_{21} , S_{23} , S_{25} , and S_{29} , respectively, in this specification. The outputs of the plurality of analog circuits 20, 22, 24, and 28 are carried by the lines 31, 33, 35, and 39, and their signals can be represented as

$$\begin{aligned} S_{31} &= F_{20}(S_{21}) + N_{20}, \\ S_{33} &= F_{22}(S_{23}) + N_{22}, \\ S_{35} &= F_{24}(S_{25}) + N_{24}, \text{ and} \\ S_{39} &= F_{28}(S_{29}) + N_{28}. \end{aligned}$$

Each of the output signals include a noise component. In the figure, the digital circuit 26 may be the major cause of the noise. The analog circuits, being proximally located to each other, experiences the same noise environment, and if

the analog circuits are identical in design, then the noise components of their respective output signals have identical values. Alternatively expressed,

$$N = N_{20} = N_{22} = N_{24} = N_{28}.$$

5 In such a configuration, one of the circuits can be assigned to be the noise separator circuit, and the separated noise signal can be used to cancel the noise components of the other output signals. In Fig. 2, the circuit 24 is used as the noise separator circuit. As discussed in Implementation 1 section above, signal S_{25} can be designed as to produce only the noise signal at the output, S_{35} , of the circuit 24. Then, the subtractor circuits 30, 32, and 38 can be used to remove the noise components of the output signals of the circuits 20, 22, and 28, respectively as follows:

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$$\begin{aligned} S_{41} &= S_{31} - S_{35} \\ &= (F_{20}(S_{21}) + N) - N \\ &= F_{20}(S_{21}); \end{aligned}$$

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$$\begin{aligned} S_{43} &= S_{33} - S_{35} \\ &= (F_{22}(S_{23}) + N) - N \\ &= F_{22}(S_{23}); \text{ and} \end{aligned}$$

20

$$\begin{aligned} S_{49} &= S_{39} - S_{35} \\ &= (F_{28}(S_{29}) + N) - N \\ &= F_{28}(S_{29}). \end{aligned}$$

Alternatively, if the noise cancellation technique as described by Implementation 2 can be implemented in the multiple analog circuit environment; however, the technique would be less effective if the input signals to the circuits,

S_{21} , S_{23} , and S_{29} , have identical values.

A Sample Implementation

Referring now to Fig. 3, an implementation of the present invention for a baseband receiver for a cellular phone product is illustrated. The desired outputs of the entire circuit 50 are the output I 67 and the output Q 69, denoted S_{67} and S_{69} respectively. Signal S_{67} is the "clean" resultant signal of the input signal I 51, S_{51} , as processed by the first circuit 52, or $F_{52}(S_{51})$. However, because of the noise, the actual output 53, S_{53} , of the first circuit 52 is $F_{52}(S_{51}) + N_{52}$. That is,

$$S_{53} = F_{52}(S_{51}) + N_{52}.$$

To eliminate the noise component of the actual output S_{53} of the first circuit 52, a noise separator circuit 56 is used to produce the noise only, and a subtractor circuit 62 is used to subtract the noise component, N , from the actual output 53, S_{53} , of the first circuit 52. In particular, the noise separator circuit 56 is fed a null, or a zero, input 55, causing the noise separator circuit 56 to produce, at its output 57, S_{57} , the noise component. That is,

$$S_{57} = F_{56}(S_{55}) + N_{56}.$$

Because $S_{55} = \text{null}$, $F_{56}(S_{55}) = 0$. And, because the noise separator circuit 56 is identical in design to the first circuit 52 and the noise separator circuit 56 is exposed to the same noise as the first circuit 52 due to its proximal location to the first circuit 52, the noise component of the outputs of both circuits are equal, $N_{52} = N_{56}$. Therefore,

$$\begin{aligned} S_{57} &= F_{56}(S_{55}) + N_{56} \\ &= 0 + N_{52} \\ S_{57} &= N_{52}. \end{aligned}$$

Then, the subtractor circuit 63 is used to subtract the noise component out from S_{53} by subtracting S_{57} from S_{53} . The output 63, S_{63} , from the subtractor circuit 62 is

$$\begin{aligned} S_{63} &= S_{53} - S_{57} \\ &= (F_{52}(S_{51}) + N_{52}) - N_{52} \\ &= F_{52}(S_{51}). \end{aligned}$$

A multiplexor 66 can be used to select between the noise-free signal S_{63} or the actual output signal S_{53} as the final output of the circuit 50. A noise-cancellation-enable line 69 can be used to switch the multiplexor 66 between the two signals.

As discussed by Implementation 3 section above, multiple circuits can share a single noise separator circuit to eliminate the noise components of their outputs. As illustrated by Fig. 3, a second circuit 60, proximal to and identical in design to the first circuit 52 and to the noise separator circuit 56, can use the output of the noise separator circuit 56 to eliminate the noise from its own output 61, S_{61} . However, the second circuit 60 requires the use of its own subtractor circuit 64 and its own multiplexor 68.

In the embodiment illustrated by Fig. 3, the first circuit 52, the second circuit 60, and the noise separator circuit 56 are delta-sigma analog-to-digital converters with digital outputs 53, 71, and 57, respectively. The noise cancellation technique can be used in for the digital or for the mixed signal environments as well as the analog environment.

For the embodiment of Fig. 3, the subtractors 62 and 64 must be digital subtractors. Digital subtractors are well known in the art, and Fig. 4A illustrates a simple digital subtractor 100. Referring to Fig. 4A, the noise 106 is negated by multiplying the value by -1 using a multiplier 102. The multiplier 102 is a very simple circuit to perform a 2's complement to the incoming signal, effectively

flipping the incoming bits. Then, the negated noise 108 is added 104 to the input 110 to obtain an output 112, the value which is the input value minus the noise value.

5 Although the present invention has been described in detail with regarding the exemplary embodiments and drawings thereof, it should be apparent to those skilled in the art that various adaptations and modifications of the present invention may be accomplished without departing from the spirit and the scope of the invention. Accordingly, the invention is not limited to the precise embodiment shown in the drawings and described in detail hereinabove. Therefore, it is intended that all such variations not departing from the spirit of the invention be considered as within the scope thereof as limited solely by the claims appended hereto.

10 In the following claims, those elements which do not include the words "means for" are intended not to be interpreted under 35 U.S.C. § 112 ¶ 6.